

Tuned to the needs of handheld and battery powered devices, the ELP-11 implements the complete TCP/IP protocol stack and associated security requirements in a low gate count, ultra-low power design that is readily integrated into either COT or ASIC design flows. The ELP-11 offers significant power dissipation advantages compared with embedded processors executing software protocol stacks. Other advantages include simplification of system integration, elimination of costly performance tuning activities associated with embedded TCP/IP and security stacks, and the liberation of scarce processor cycles for value-added, end-user oriented processing.

Two related phenomena arise in wireless embedded and handheld devices built for today's high speed cellular and WLAN networks. First, the amount of processing required per bit of communication becomes prohibitive as data rates increase (MIPS/Mbps). This situation is made even worse by the much higher bit error rates in wireless environments. Second, the energy required to perform that processing is a serious drain that shortens battery lifetimes, limiting the availability and usefulness of these devices (mW/Mbps).

Overcoming Battery Life Issues

The traditional approach to networking and security protocol processing in embedded devices has been to deploy a software implementation running on an embedded RISC or DSP core. This approach has been appropriate for low data rate connections, but starts to break down at even relatively modest data rates (e.g. 128 Kbps 1xRTT, 384 Kbps 3xRTT) available on 2.5G and 3G cellular networks. At much higher WLAN data rates (54 Mbps 802.11a and g, and proprietary "turbo" extensions to data rates approaching 100 Mbps) this processing consumes excessive energy and makes battery life unacceptably short (see Figure 1). In most cases, devices lack sufficient processing capacity – even at maximum clock rate – to make use of the data rates available on the communication channel.

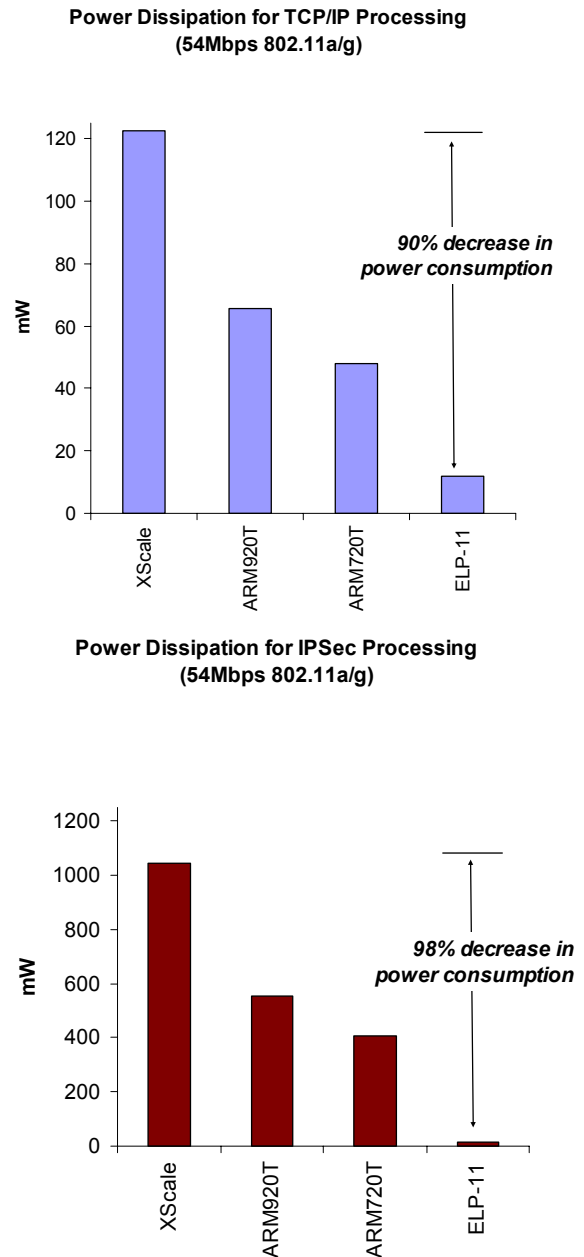


Figure 1: Power dissipation for wireless protocol processing

Wireless networks also represent unique challenges for the common TCP/IP network protocols, which were originally designed for wired networks. Bit error rates on wireless networks are three orders of magnitude higher than on modern wired networks, resulting in much higher rates of dropped and duplicated packets and out-of-order packet arrival. These transmission problems represent wasted energy in the mobile device as no useful information is conveyed in these data packets while consuming processing resources. As signal levels drop in fringe areas or as batteries come to the end of their useful life, these events becomes much more frequent, further increasing processing demand (and therefore energy consumption). Energy consumption, per bit of useful data, is much worse in wireless environments than in a wired network at the same rate of data throughput.

Elliptic Semiconductor's ELP-11 offers power-optimized network and security protocol offload engines that solve the mobile energy problems.

The ELP-11 offering consists of two major modules: the TCP/IP Offload Engine (TOE) module provides complete internet communication protocol processing; and the Security Protocol Processor (SecPP) module provides security protocol processing, implementing both IPSec and SSL/TLS, while providing support for other security protocols such as 802.11i. This focus on complete protocol processing is unique in the industry, and provides both power and complexity reduction benefits to users. By design, these modules work efficiently together, but can also be separated to provide either the networking component or the security component separately.

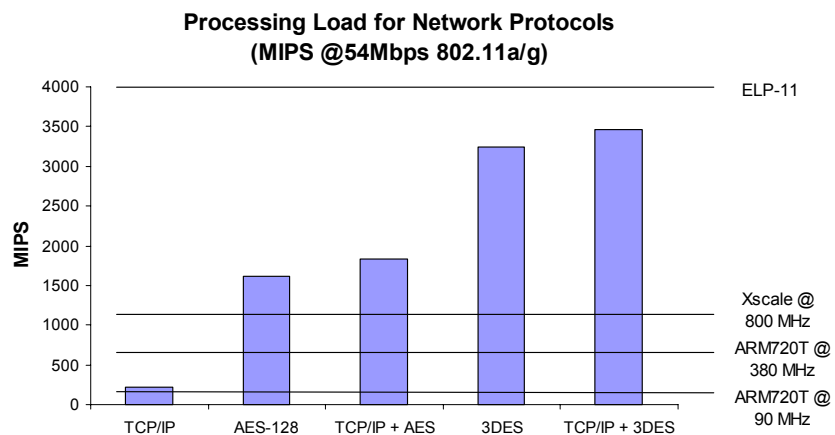


Figure 2: Processing Demands for Common Protocols

Tuned Hardware for Mobile Platforms

Analysis of performance for a software implementation in a host application processor is shown in Figure 2. The x86 and XScale data was obtained using instrumented versions of some widely available software stacks built for the two commonly available processor families. The XScale processor family is representative of a state-of-the-industry embedded ARM design, and is being widely deployed in embedded applications such as the PocketPC. General purpose processors are inherently inefficient at these tasks because of the need to transport the data back and forth between various resources: memory, ALUs, and registers. Data transfers of these types involve movement of large amounts of data across power hungry buses. In the embedded environment, roughly four processor cycles are required per bit transmitted for TCP and IP protocol

termination on the ARM-based XScale. This metric translates well to the common ARM9 and older ARM7 families.

Cryptographic protocol processing involving both cipher and secure hash (MD5) computation is also shown. AES is a moderately computationally intensive cipher algorithm, selected by NIST as a replacement for the aging DES for its security and its suitability to implementation in both hardware and software. In the XScale, this algorithm requires about 35 instructions per bit. Triple DES cryptography is an even larger load on the CPU, requiring about 60 instructions per bit versus.

This translates directly to higher power consumption. Figure 3 shows power demand for the popular ARM families of embedded application processors. Clearly as data rate increases, the various processor solutions fail to keep up, becoming the limitation on usage of available bandwidth. By comparison, the ELP-11 requires only 16 mW at a full 54 Mbps data rate. Elimination of this computational load from the application processor frees up the processor to do useful work, or affords the system designer the opportunity to select a smaller, cheaper processor.

Fortunately, TCP/IP and the various security standards are mature, and change relatively infrequently. As a result, major portions of those standards can be implemented in hardware with little concern about

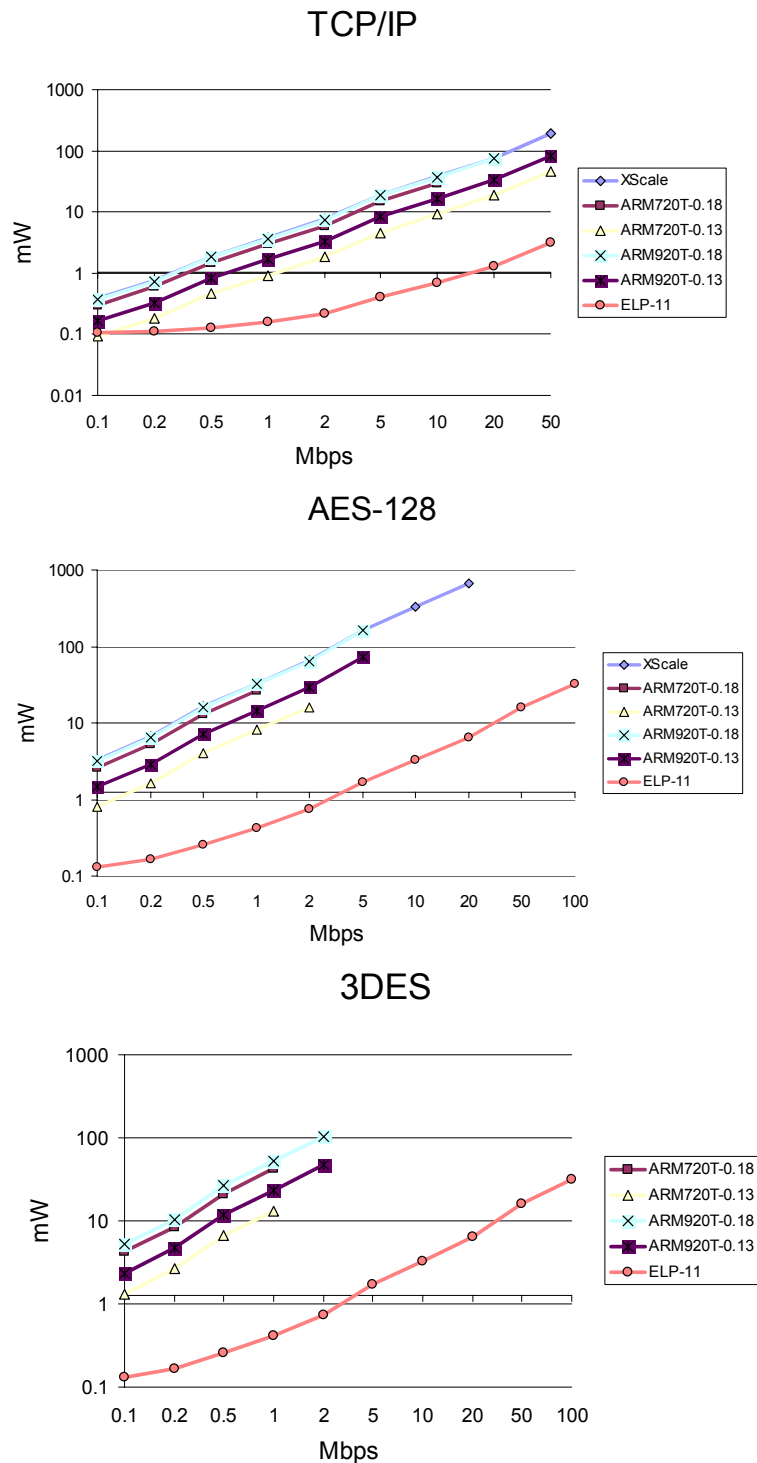


Figure 3: Power consumption vs data rate

protocol changes. The ELP-11 incorporates a task engine, which receives its microcode at boot time. This permits standards or protocol revisions to be addressed within the context of the ELP-11.

The bottom line – it’s a simple matter of physics. Battery life is directly proportional to the number of gates being clocked to complete a given transaction. With a fully tuned, dominantly hardware design, both the clock speed and data-path are tuned to minimize the power consumption. The next section of this paper explores some of the mechanisms Elliptic uses to achieve this dramatic performance improvement.

Low Power Implementation Techniques

Low power design starts with careful consideration of data transformations required at each stage of processing and the data and control flows to move a packet from source to destination.

For the ELP-11, shown in Error! Reference source not found., the guiding principle was to transform data as completely as possible with each move and leave it in place as long as possible once located in the packet buffer memory (PBM). This has resulted in a patent-pending architecture in which data remains where it was first moved to when sourced from either the application or MAC/baseband layers. The PBM consists of multiple blocks of standard embedded memory of the designer’s choice, typically custom compiled 6T SRAM. Arbitration/contention controllers provide apparent multi-ported access to the PBM, and memory blocks may be individually powered or placed in stand-by to provide variable power/bandwidth trade-offs.

Memory can be sized to accommodate the needs of different end-user devices, ranging from 8 KB for simple e-mail (IMAP/POP/SMTP) and web-browsing applications (HTTP) up to 128 KB for bi-directional streaming media for VoIP and video applications. DMA engines responsible for transferring data from host or MAC processor perform pre-fragmentation, CRC computation, and other routine operations on-the-fly. CRC checks for inbound packets from the MAC layer are performed during the DMA operation, allowing corrupted packets to be dropped immediately. The final phase of inbound datagram reassembly is performed

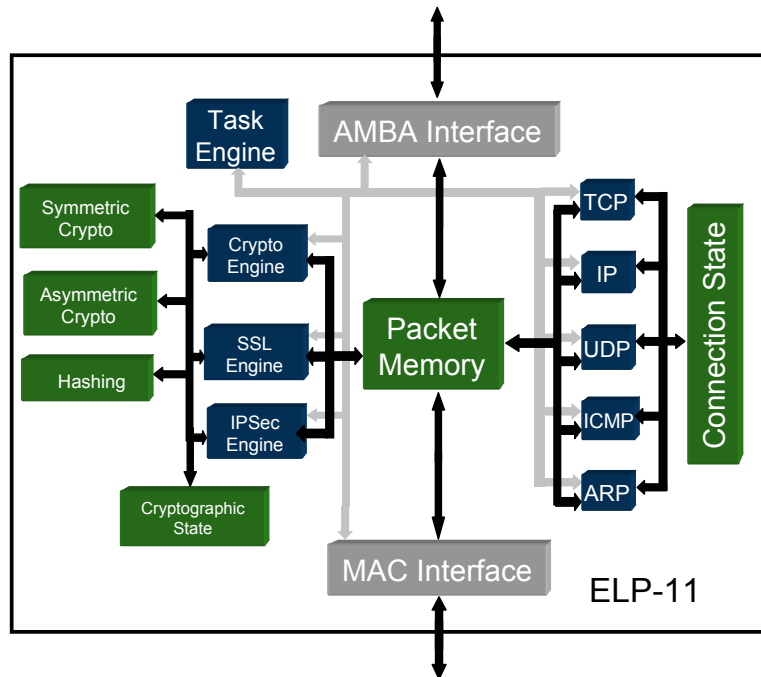


Figure 4: ELP-11 Block Diagram

automatically by the scatter/gather DMA engine.

Clock distribution and management is another key power consumption control feature. A patent-pending policy manager distributes clock control and management throughout the ELP-11 to dynamically optimize power consumption and throughput. As usual, various protocol engines are clocked only when required. The central task engine schedules packets for processing in required protocol engines and enables the clock to these engines. Engines automatically gate their clocks off and revert to stand-by when scheduled tasks are completed. The task engine similarly reverts to stand-by when all available packets have been scheduled.

The task engine is used only to control the sequencing of data through the protocol engines; these engines manage their own access to packet data stored in the PBM. The policy manager supports selection of different clock control policies according to instantaneous system and network traffic conditions, allowing different throughput vs. power consumption tradeoffs according to traffic content, for example. Protocol changes, extensions, and even custom protocols are attained by reprogramming the task engine microcode. Microcode for standard protocols is supplied as part of the product, and customers do not ordinarily program the task engine microcode.

The ELP-11 also makes use of a variety of industry-standard power-management techniques to deliver a very low-power solution. While the largest gains in power consumption reduction come from careful architectural design, there are a variety of “black art” techniques that contribute to reduced power consumption. These vary in complexity, difficulty during design, and dependence on fabrication process. Among these techniques are the following:

Cycle and gate reduction from tuned hardware. This is essentially a continuation of architecture definition to the micro-architecture of individual functional units. Modern EDA environments typically include high-level options to optimize for area, speed or power. While capable of modest improvements in power consumption (typically 5-10%), far greater gains are possible through interaction of the designer to constrain and guide the tools. In this scenario, gains of 15-25% are typically achievable, although much larger gains can be obtained in some fortunate circumstances. These large gains typically occur from skillful conversion of a function to a canonical form, as may be found in some cryptographic processing, for example.

Multiple V_t libraries. With the push to 130 nm and beyond, static leakage currents are an increasingly important component of overall power consumption, particular for SRAM memory blocks in sleep mode. It is common for sleep mode power consumption to be worse for a given memory in 130 nm technology than for the same memory in 180 nm technology. This has given rise to a need for libraries with multiple implementations of the same cells using transistors having different V_t s. Low V_t cells are used where maximum performance is required or static power consumption is not of concern. High V_t cells are used where sleep mode power consumption must be minimized. The ELP-11’s “low-and-slow” approach limits maximum clock rates to about 50 MHz, making it possible to close timing using high V_t cells throughout.

Multiple and/or variable V_{DD} domains. Similar to the multiple V_t libraries, aggressive power management strategies for SoCs can use on-chip or off-chip power conversion circuitry to reduce V_{DD} levels to reduce both static and dynamic power consumption. As above, the tradeoff is between speed and power consumption. ELP-11's design approach can again successfully take advantage of an advanced V_{DD} management strategy to produce additional power savings.

Clock domain partitioning and gating. Another feature of modern EDA tools is automatic generation of clock domains and gating of individual domains. Automatically generated clock domains tend to be fairly coarse, resulting in limited opportunities for power conservation. While useful for reducing power consumption in systems that have major functions that are used infrequently, the ELP-11's internal clock gating and tuned domain partitioning provides much finer control, ensuring that the minimal set of circuitry required to achieve a particular function is active only when needed.

Interconnect and parasitic reduction. As active device geometries continue to push to smaller dimensions and automated EDA tools are increasingly relied on to manage ever higher levels of complexity, interconnect and parasitic capacitances come to dominate timing closure and dynamic power consumption. ELP-11 modules supplied as hard macros are carefully laid out to localize functionality as much as possible, and therefore minimize power losses in interconnect and parasitics.

Minimum power consumption is achieved by matching hardware and microcode to minimize the use of circuitry consistent with performance requirements, and to modularize and regularize hardware to provide support for techniques such as clock gating. Doing so means taking a system-level view of the problem beyond the functions provided within the module, to examine how the modules are used by real applications in real networks and providing hardware and microcode to achieve overall system objectives. Optimal designs may vary dramatically depending on the system context (e.g. traffic patterns). It is also essential to balance additional control complexity required to achieve the power savings with the value of the power savings. As in many things, there may be 10% gain for 80% cost, and it may be best to stop there.

Summary

A unique focus on holistic protocol processing combined with skilled IC design from a veteran team with years of SoC experience allows Elliptic Semiconductor to deliver reliable, highly tuned hard and soft macro IP to satisfy the most critical power and throughput requirements.

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